Investigation of a Digital Non-Foster RC Circuit Using Pade and Prony Approximations

Sunny Arokia Swamy Bellary, Nelyadi S. Shetty, Ryan C. Hill, Thomas P. Weldon and James M. Conrad

University of North Carolina at Charlotte

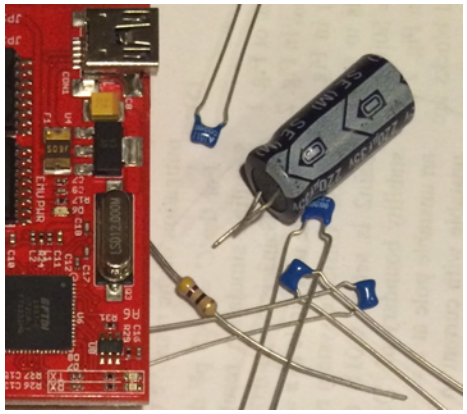
Overview of Presentation

- Overall Goal
  - Use Pade and Prony methods to implement digital non-Foster devices (such as negative capacitance)
- Review Prior Analog non-foster approaches
  - Analog non-Foster background
- New Digital RC Circuits
  - Theory & Prior Backward Difference Approach
  - New Proposed Pade and Prony Approximations
    - Theoretical Results
    - Measured Results

Analog Non-Foster Background

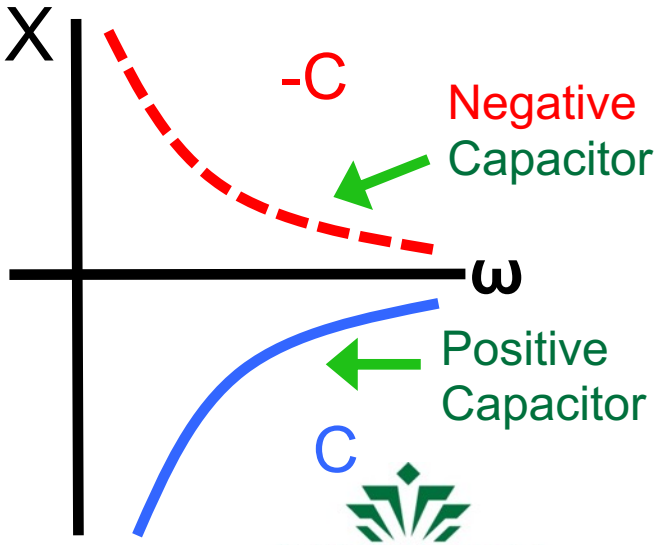
Non-Foster Circuits: What are They?

- "Normal Circuits"
  - Key passive devices
    - Resistors: R
    - Capacitors: C
    - Inductors: L
  - Used just about everywhere in electronics



Reactance

- Non-Foster Circuits
- Of primary interest here
  - Negative Capacitors
  - Negative Inductors
    - Everything is "flipped"
    - Enables wide bandwidth



Why Digital Non-Foster?

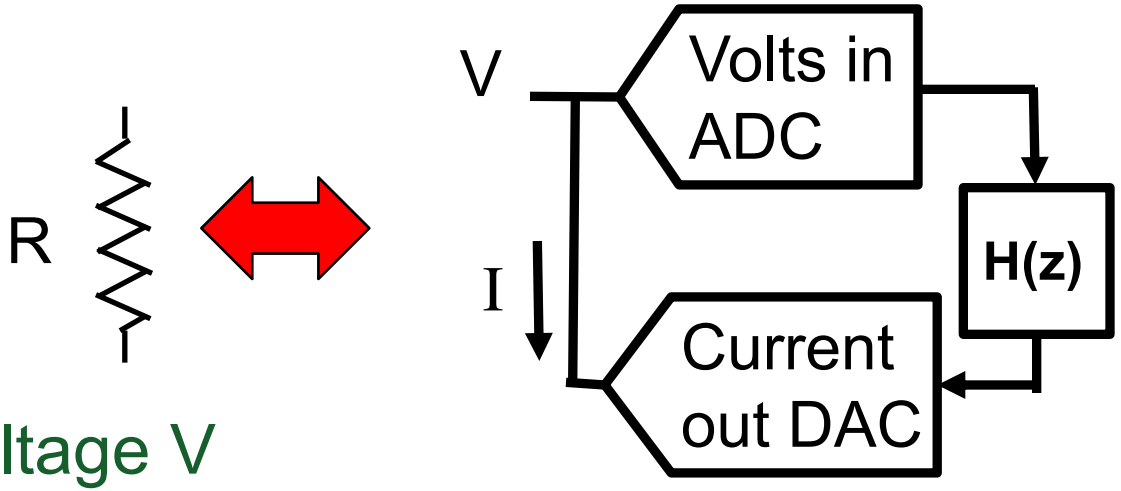
- Several problems with analog implementation
  - Instability
  - Component tolerances
  - Configurability
  - Compatibility with digital IC processes

- Solution: digital non-Foster
  - Repeatability and control of digital tech. improves stability
  - Potential for digitally/software tunable/adaptive

- Today: The design of a digital Non-Foster RC series circuits using Pade and Prony indirect modelling methods.
  - Implementation Prototype

What is Digital Non-Foster?

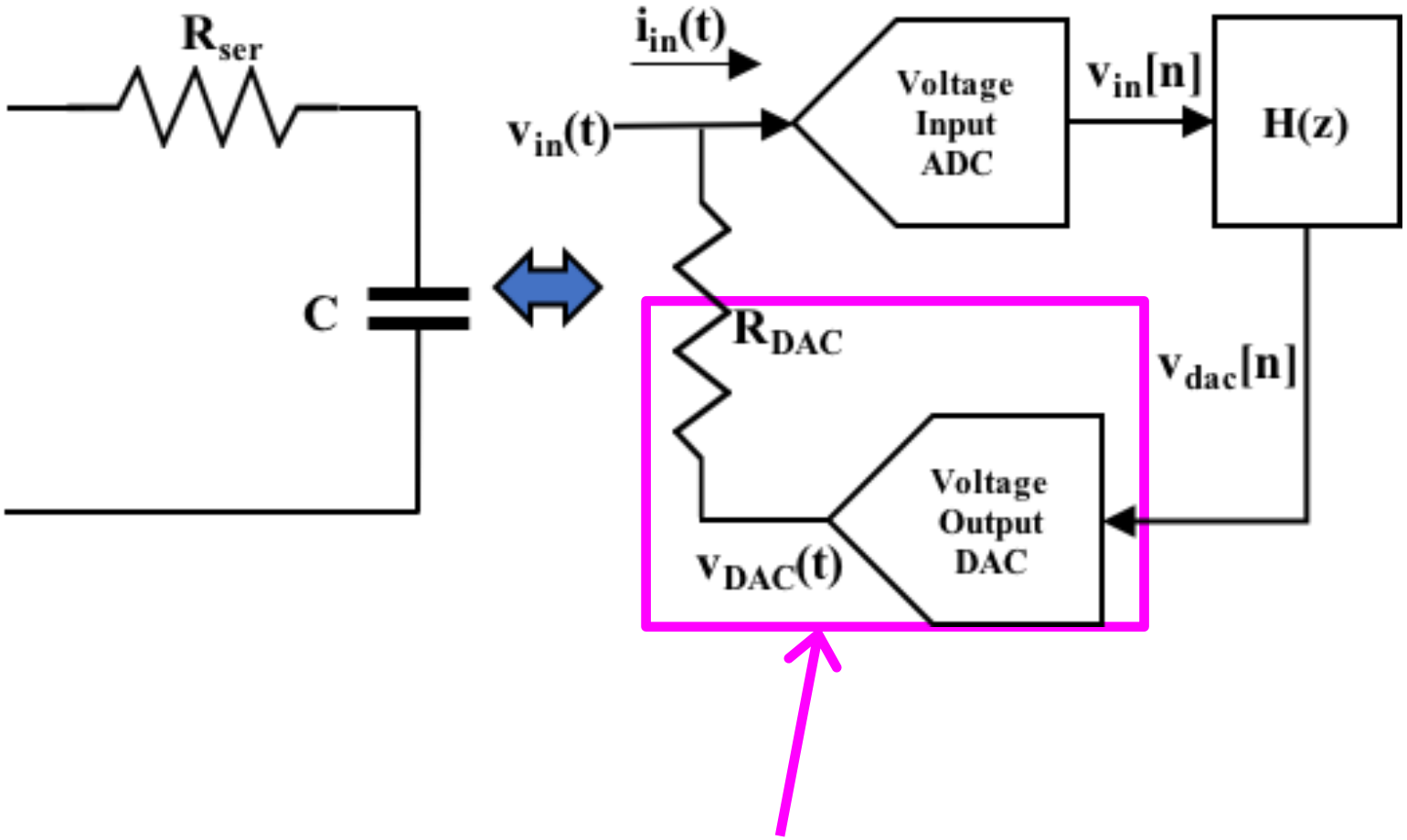
Simple Example: Digital Resistor



- Measure voltage V
- Set current I
- Let H(z) = 1/R
- So, DAC current: I = V/R

… yields world's most expensive resistor!
… but is tunable
... Useful in implementing exotic impedances

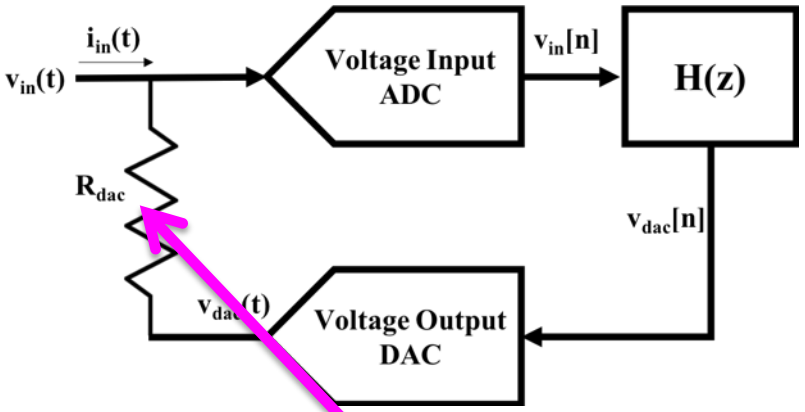
Digital non-Foster Thevenin Form



- DAC source plus R_{dac} is a Thevenin source
- H(z) determines impedance behavior

Theory: Digital non-Foster Impedance

- Measure v(t) ADC: v[n] = v(nT)
- Calculate $v_{dac}[n]$ H(z): $v_{dac}[n] = v[n]*h[n]$
- Set $i_{in}(t)$ DAC: $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$



$$V_{dac}(s) = V_{in}^{*}(s)H(z)\frac{(1-z^{-1})}{s}\Bigg|_{z=e^{sT}}$$

$$V_{dac}(z) = H(z)V_{in}(z)$$

$$I_{in}(s) = \frac{V_{in}(s) - V_{dac}(s)}{R_{dac}}$$

$$V_{in}^{*}(s) = \sum v_{in}(nT)e^{-nsT}$$

$$= \sum V_{in}(s - n\omega_0)/T$$

Input impedance is then:

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \frac{sTR_{DAC}}{sT - H(z)(1-z^{-1})}\Bigg|_{z=e^{sT}}$$

(Starred Transform)

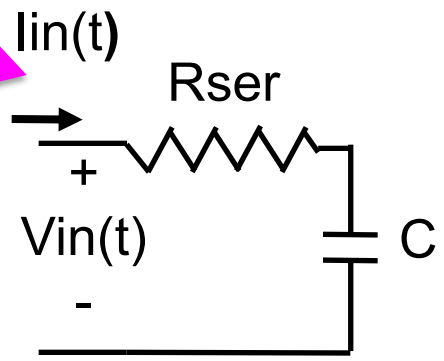
Prior Backward Difference Method

Digital RC Circuits

Theory: Digital Non-Foster RC Circuit

Analog series RC circuit with series resistance Rser:

$$v_{in}(t) = i_{in}(t)R_{ser} + \int \frac{i_{in}(t)dt}{C}$$



Taking the derivative:

$$\frac{dv_{in}(t)}{dt} = R_{ser}\frac{di_{in}(t)}{dt} + \frac{i_{in}(t)}{C}$$

Assuming:

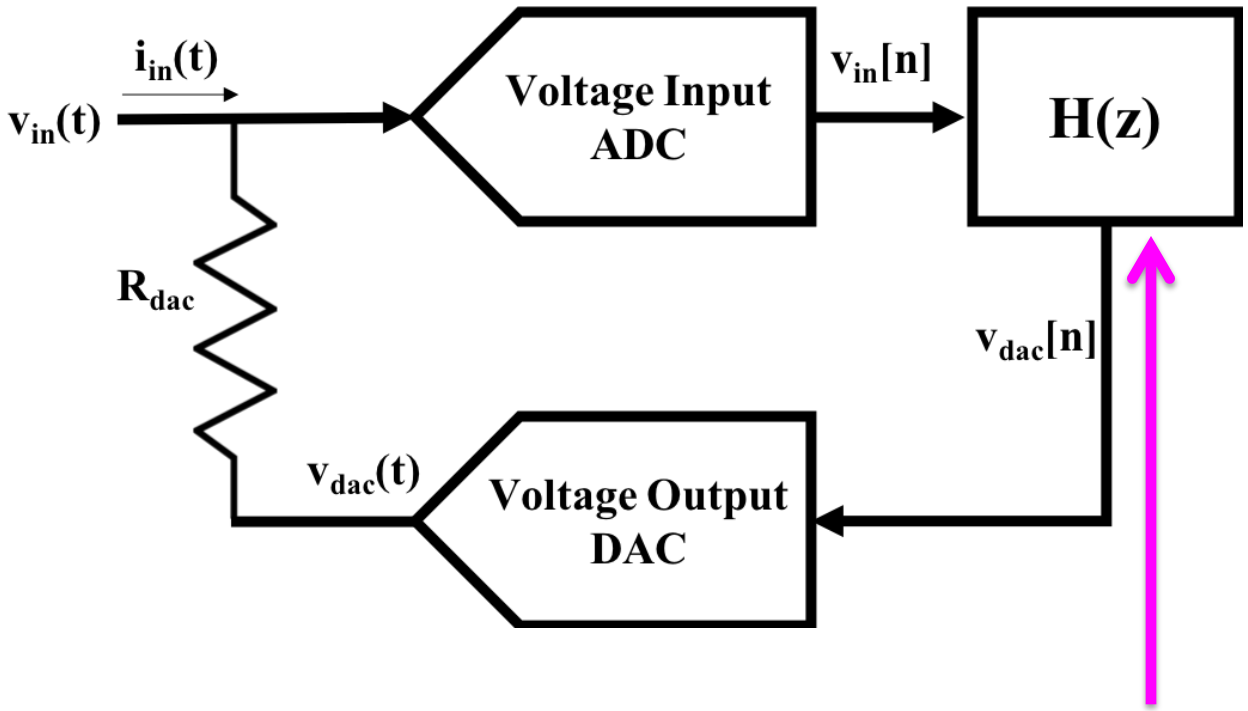
$$\frac{dv_{in}(t)}{dt} = \frac{v_{in}[n] - v_{in}[n-1]}{T} \qquad i_{in}[n] = \frac{v_{in}[n] - v_{dac}[n]}{R_{dac}}$$

Yields:

$$v_{dac}[n](R_{ser}C + T) = v_{in}[\mathrm{n}](R_{ser}C - R_{dac}C + T)$$

$$+v_{in}[n-1](R_{dac}C - R_{ser}C) + v_{dac}[n-1]R_{ser}C$$

Theory: RC Circuit Transfer Function



Taking the z transform to solve for H(z):

$$H_{RC}(z) = \frac{V_{dac}(z)}{V_{in}(z)} = \frac{(R_{ser}C - R_{dac}C + T)z + (R_{dac}C - R_{ser}C)}{(R_{ser}C + T)z - R_{ser}C}$$

Where Rser and C can be negative

Why Signal Modelling Techniques over Backward Difference

Backward Difference

- Approximates derivative
- Imperfect approximation

Signal Modelling Techniques

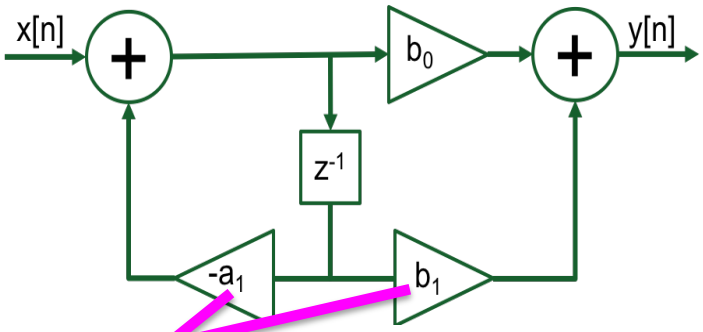
- General-purpose, least-square approach
- Approximate and model desired impedance
- Order of system can be decided based on requirements
- Modelling techniques perfectly matches the first few points

Proposed Pade Design Method

Digital *RC circuits*

Theory: Pade Design for RC Circuit

Pade approximation method is a form of indirect modelling



$$H(z) = Z(h[n])$$

In the Pade Method:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{B(z)}{A(z)} = \frac{\sum_{m=0}^{N_B}(b_m z^{-m})}{1+\sum_{n=1}^{N_A}(a_n z^{-n})} \approx \sum(g[n]z^{-1}) = G(z)$$

where g[n] is the desired impulse response, X(z)=1 and Y(z)≈G(z), then B(z)X(z)=A(z)Y(z)≈A(z)G(z) results in the Pade Approximation form

$$B(z) = \mathrm{A(z)\,G(z)}$$

Theory: Pade Design for RC Circuit

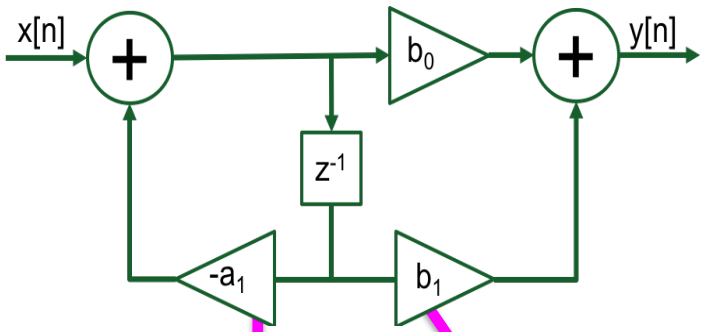
$$B(z) = \mathrm{A}(z)\,\mathrm{G}(z)$$

After taking inverse z-transform on both sides:

$$\sum_{k=0}^{N_A} (a[k]g[n-k]) = b[n] \quad where \quad a_0 = 1$$

Pade method exactly matches first few points of h[n] to g[n] by solving for the filter coefficients. In matrix form, the Pade method involves finding solution for A and B such that:

$$\bar{\bar{G}}\,\bar{A} = \bar{B}$$



Our Pade approximation exactly matches three points then:

$$\bar{\bar{G}}\,\bar{A} = \begin{bmatrix} g[0] & 0 \\ g[1] & g[0] \\ g[2] & g[1] \end{bmatrix} \begin{bmatrix} 1 \\ a_1 \end{bmatrix} = \bar{B} = \begin{bmatrix} b_0 \\ b_1 \end{bmatrix}$$

where the filter coefficients a_1, b_0 and b_1 are solved for using Pade procedure

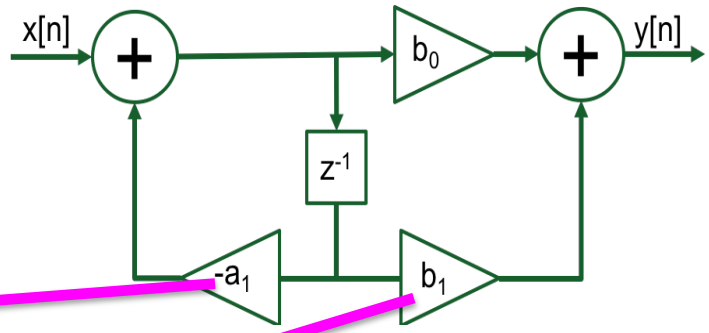
Proposed Prony Design Method

Digital *RC circuits*

Theory: Prony Design for RC Circuit

Prony method forms a solution A and B by minimizing the square error over a variable number of points of g[n], instead of exactly matching the first few points of g[n].

Prony method has zero error in approximating g[n] by h[n], but typically has error for subsequent points.



For eight points of g[n], the Prony method yields:

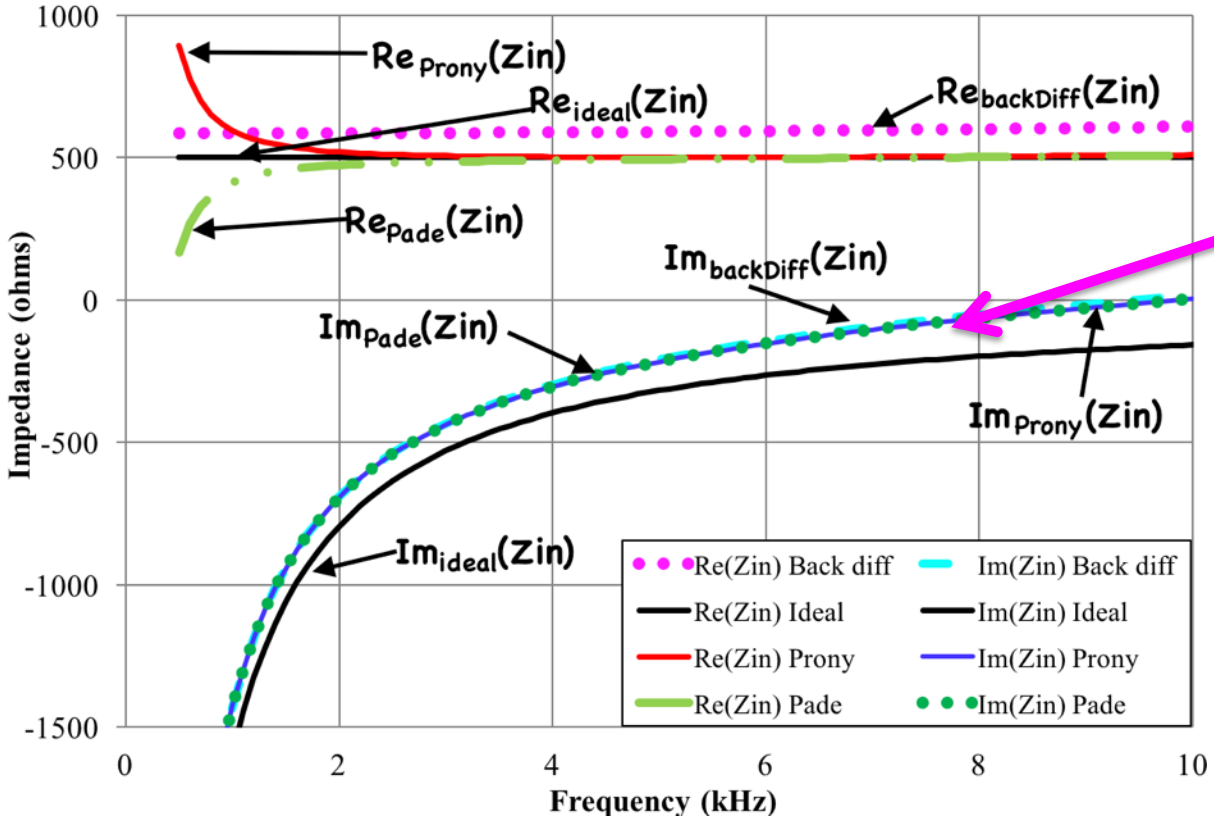
$$\bar{\bar{G}}\,\bar{A} = \begin{bmatrix} g[0] & 0 \\ g[1] & g[0] \\ \vdots & \vdots \\ g[7] & g[6] \end{bmatrix} \begin{bmatrix} 1 \\ a_1 \end{bmatrix} \approx \begin{bmatrix} b_0 \\ b_1 \end{bmatrix} = \bar{B}$$

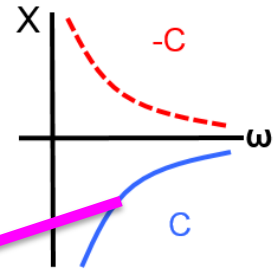
where the filter coefficients a_1, b_0 and b_1 are solved for using a least squares Prony procedure

Measured Results

RC Circuits

RC Measurements





Rser = 500 ohms

C = 0.1 μF

R_{DAC} = 1000 ohms

T = 20 μs

Prony Performs better

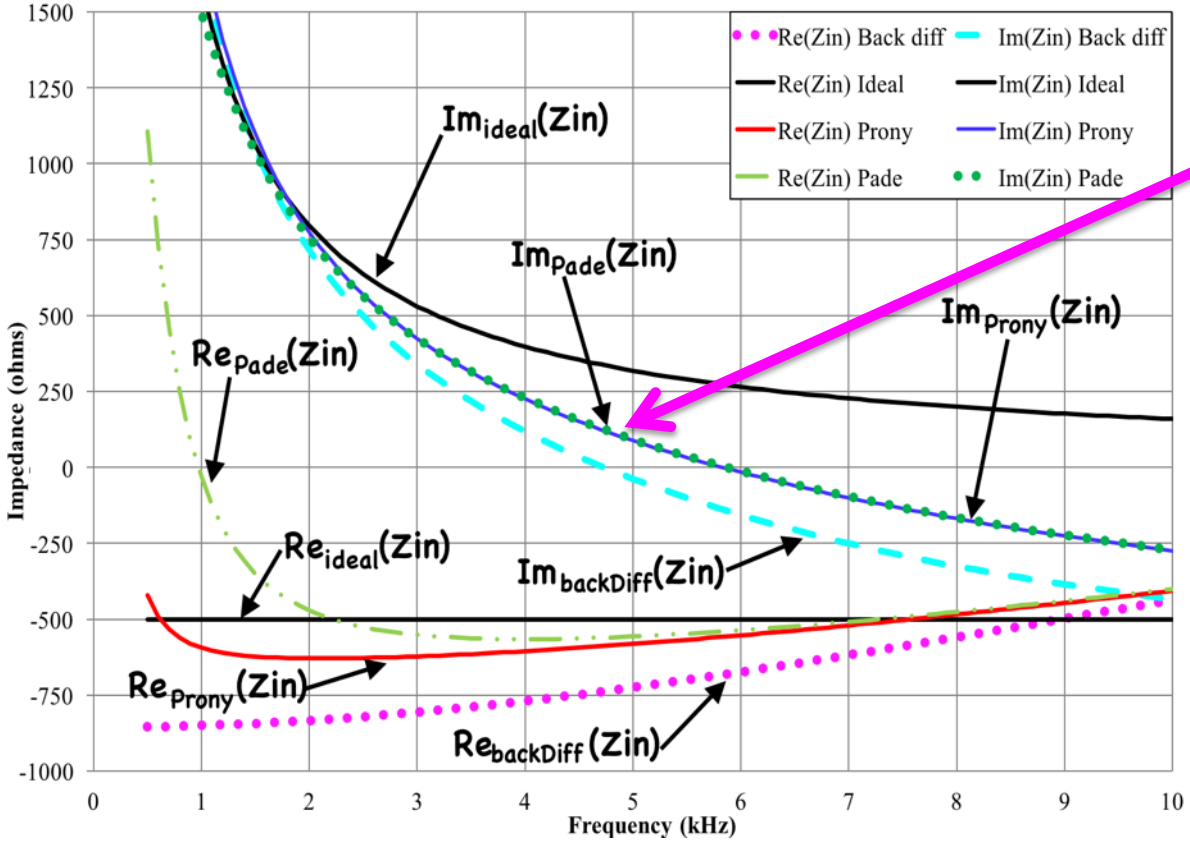
$$Z_{inIdeal}(s) = R_{ser} + \frac{1}{sC}$$

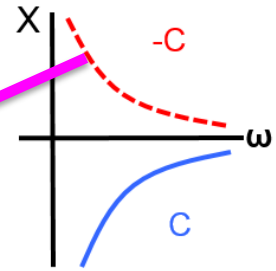
Rser = 500 ohms C = 0.1 μF

$$H_{Prony}(z) = \frac{-z + 1.2523}{z - 0.7523}$$

$$H_{Pade}(z) = \frac{-z + 1.2788}{z - 0.7788}$$

RC Measurements





- **Rser = -500 ohms**
- C = -0.1 μF
- R_{DAC} = 1000 ohms
- T = 20 μs

Prony Performs better

$$Z_{inIdeal}(s) = R_{ser} + \frac{1}{sC}$$

Rser = -500 ohms C = -0.1 μF

$$H_{Prony}(z) = \frac{3z - 2.7570}{z - 0.7523}$$

$$H_{Pade}(z) = \frac{3z - 2.8364}{z - 0.7788}$$

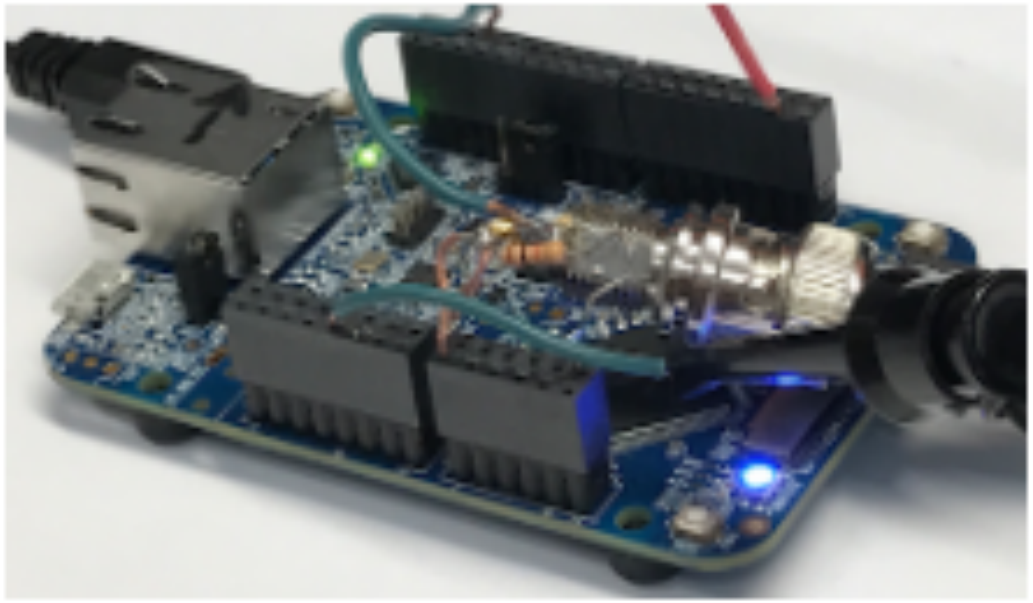
Comparison of Pade and Prony Approximations

Pade	Prony
Pade Method forms a pole-zero model by exactly matching the first few points of the indirect model	Prony method forms a pole-zero model by minimizing the square error over a number of points
Model doesn't guarantee stability	Some Models of all pole Prony models guarantee stability
Output is perfectly matched for the first N_A+N_B+1 points	Output is perfectly matched for greater than N_A+N_B+1 points

Implementation Results

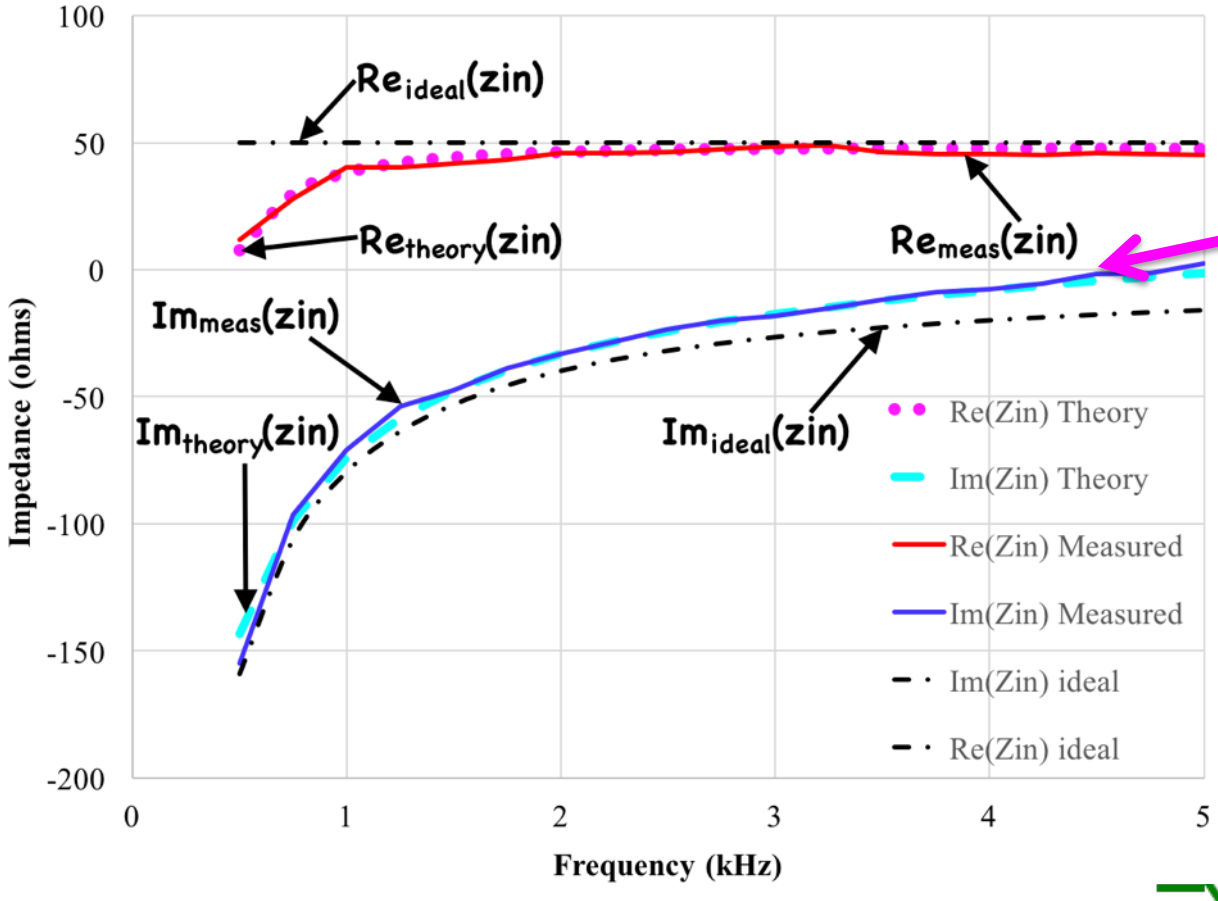
Digital RC Circuits

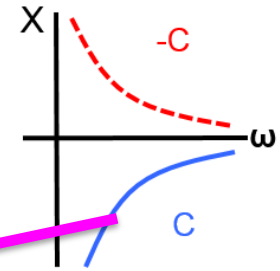
Prototype



- FRDM-K64F ARM embedded board
- ADC~1 MHz
- DAC~1 MHz
- MCU Clock ~ 120 MHz

Prony RC Implementation





- **Rser = 50 ohms**
- C = 2 µF
- R_{DAC} = 1000 ohms
- T = 20 µs

Rser = 50 ohms C = 2 µF

$$H_{Prony}(z) = \frac{-19z + 19.5502}{z - 0.8184}$$

$$Z_{inIdeal}(s) = R_{ser} + \frac{1}{sC}$$

Summary

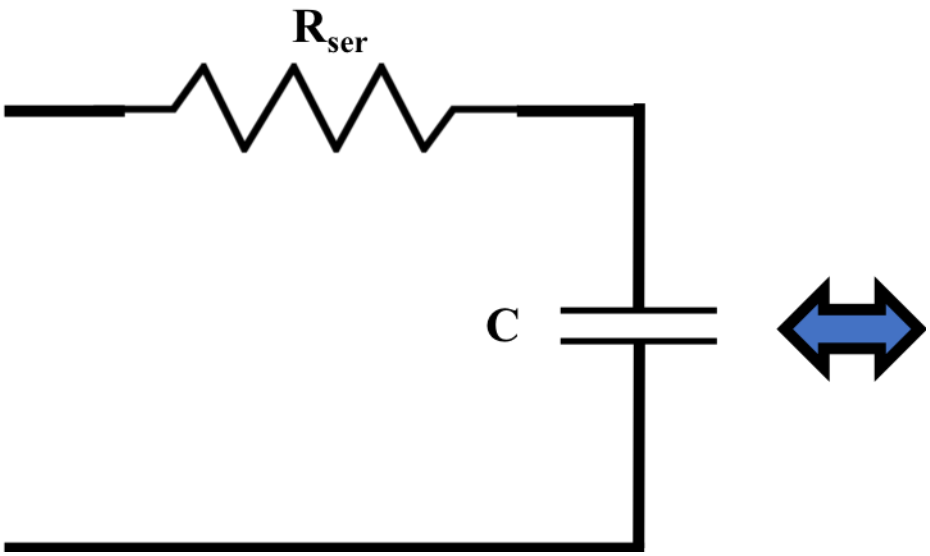
- Pade and Prony methods
  - compared to a previous backward difference for digital RC
- Pade vs Prony
  - Both closely matched the desired resistance at the mid-band range
  - Both reactance of closely matched the backward difference
  - Pade resistance very high at low frequency
  - Prony design closely matches the predicted theoretical design
- Pade & Prony give designer two new design tools beyond prior backward difference methods

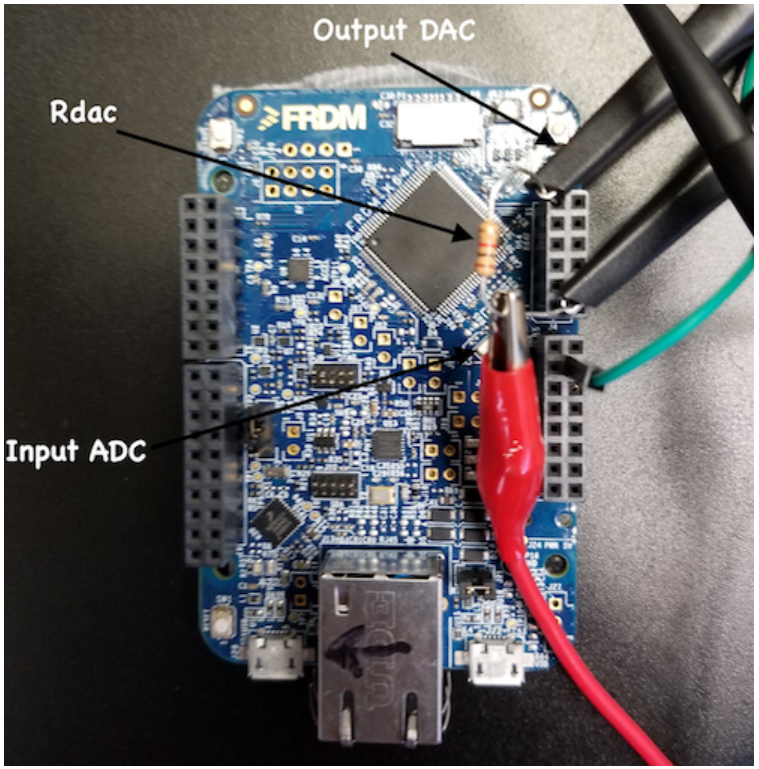
Related and Upcoming Work

Related Work

- Positive and Negative Digital RLC Circuits
- Different Signal modelling techniques to get better approximate results

Thank You!





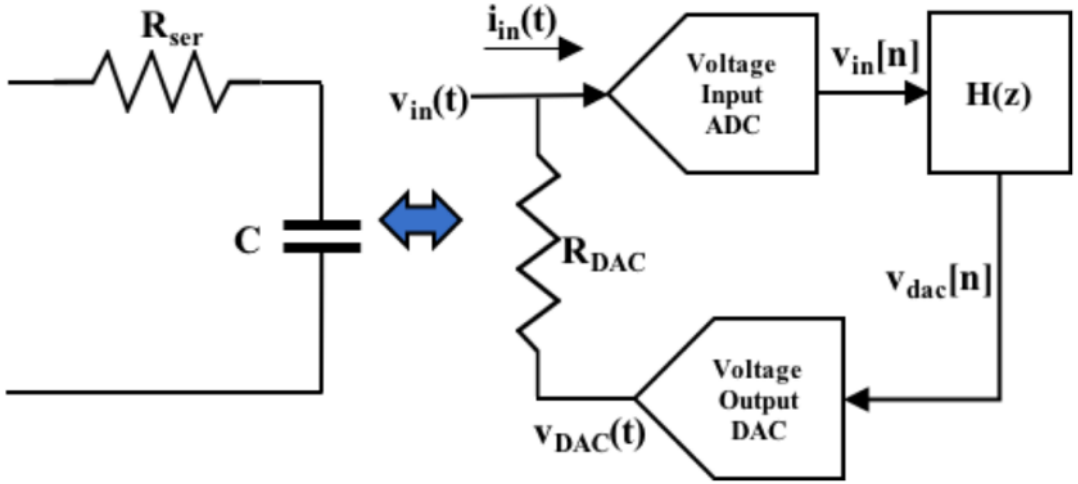
Questions?

BACK-UP Slides

Classical Digital Filter Design Methods

- Start with Analog filter design and convert to a digital filter
- Some of the methods are
  - Impulse Invariance Methods
    - Suffer from Aliasing
  - Bilinear Transform Methods
    - Map z-plane into s-plane (wrapped)

Prior Backward Difference Method



- ADC with clock period T digitizes the analog input voltage signal vin(t) creating a discrete-time signal $v_{in}[n] = v_{in}(nT)$
- The DAC input of the output of digital filter H(z) is then

$$v_{DAC}[n] = h[n] * v_{in}[n]$$

where H(z) is the z-transform of impulse response h[n] in the convolution above

- Design goal is to find H(z) that produces the desired analog impedance at $v_{in}(t)$ corresponding to the analog circuit
- For RC circuit,

$$v_{in}(t) = i_{in}(t)R_{ser} + \frac{1}{C}\int i_{in}(t)dt$$

Differentiating with respect to time yields

$$\frac{dv_{in}(t)}{dt} = R_{ser}\frac{di_{in}(t)}{dt} + \frac{1}{C}i_{in}(t)$$

Applying the backward difference approximation, gives

$$\frac{dv_{in}(t)}{dt} \approx \frac{v_{in}[n] - v_{in}[n-1]}{T} \quad \text{and} \quad i_{in}[n] \approx \frac{v_{in}[n] - v_{DAC}[n-1]}{R_{DAC}}$$

This results in Backward difference approximation

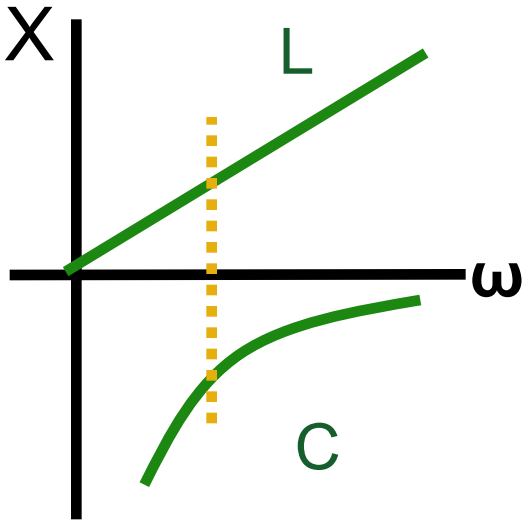
$$H_{RC}(z) = \frac{V_{DAC}(z)}{V_{in}(z)} = \frac{(R_{ser}C - R_{DAC}C + T)z + (R_{DAC}C + R_{ser}C)}{(R_{ser}C + T)z - (R_{ser}C)}$$

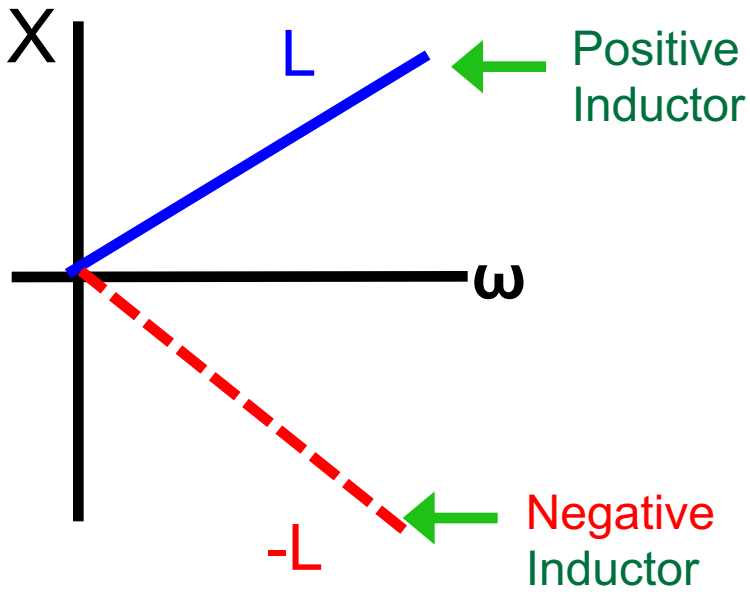
The impedance of non-Foster circuit is given by

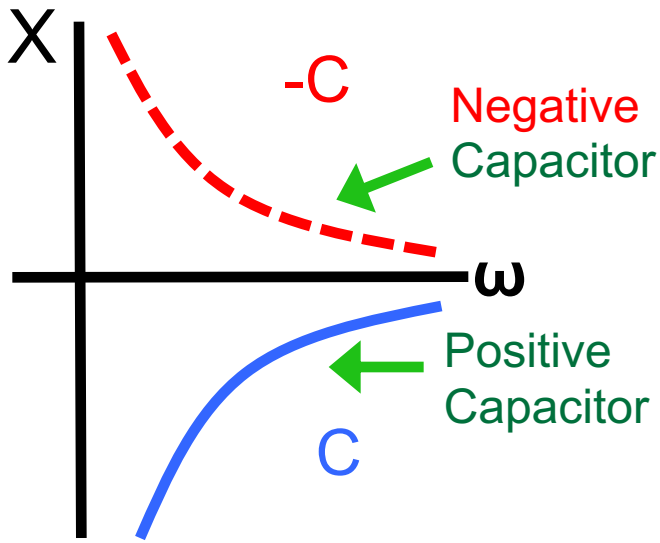
$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \left.\frac{sTR_{DAC}}{sT - H(z)(1 - z^{-1})}\right|_{z=e^{sT}}$$

Why Non-Foster Circuits?

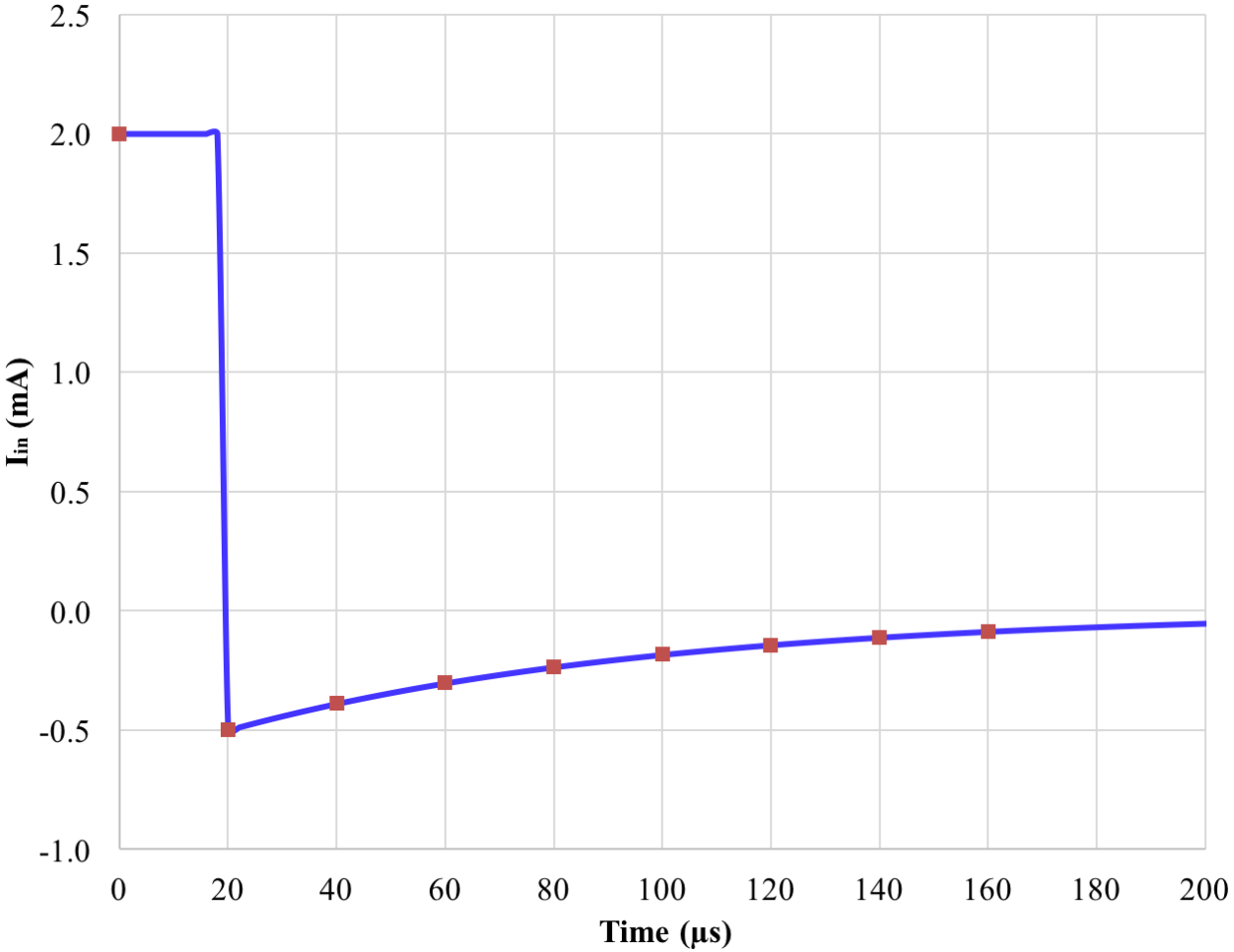
- Of particular interest:
  - Negative capacitors
  - Negative inductors





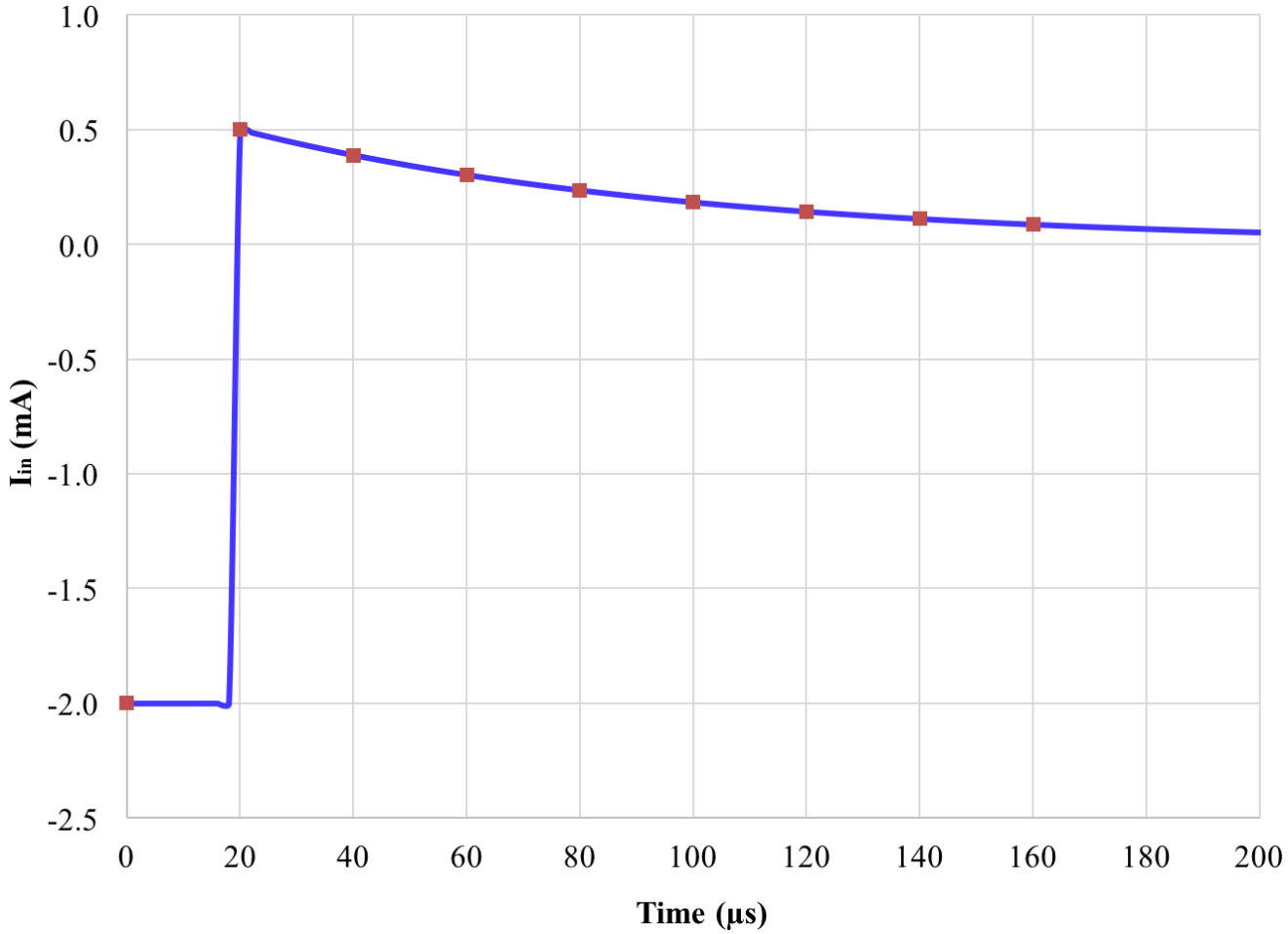


Current Points for positive RC circuit



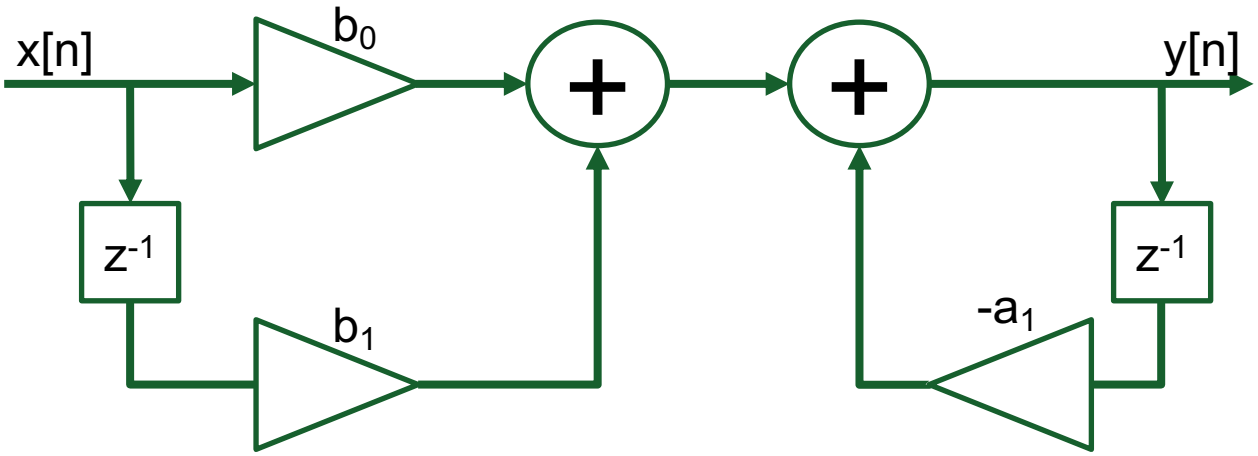
Current $i_{in}[n]$ for Rser= 500 ohms, C= 0.1µF and T=20µs. Blue curve is continuous-time current, red dots are discrete-time current samples $i_{in}[n]$

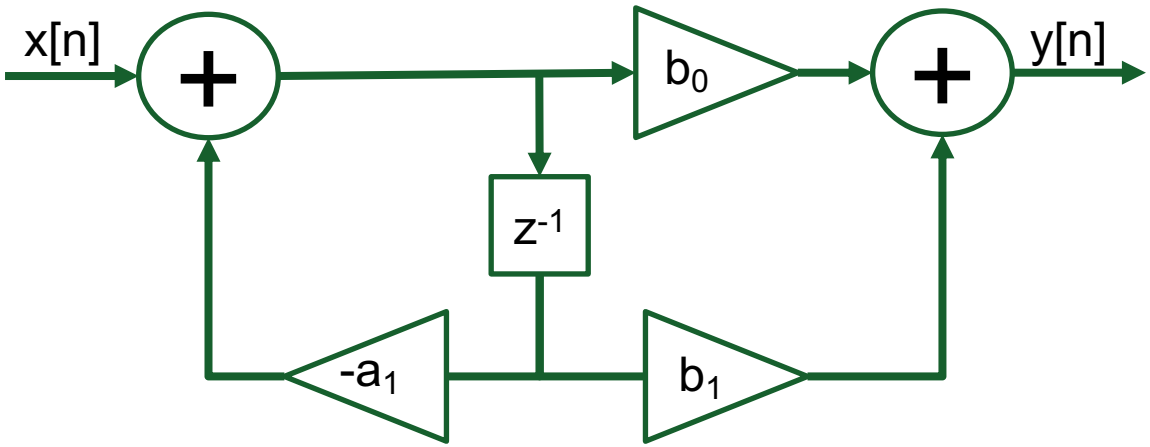
Current Points for negative RC circuit



Current $i_{in}[n]$ for Rser= -500 ohms, C= -0.1µF and T=20µs. Blue curve is continuous-time current, red dots are discrete-time current samples $i_{in}[n]$

Block Diagram





References

- N. Zhu and R. W. Ziolkowski, “Active metamaterial-inspired broad bandwidth, efficient, electrically small antennas”, *IEEE Antennas and Wireless Propagation Letters,* vol. 10, pp. 1582-1585, 2011.
- Keum-Su Song and R. G. Rojas, “Non-Foster impedance matching of electrically small antennas”, in *2010 IEEE Antennas and Propagation Society International Symposium*, Jul 2010, pp.1-4.
- R. Fleury, D. Sounas and A. Alu, “An invisible acoustic sensor based on parity-time symmetry”, *Nature Communications,* vol. 6:5905, pp. 1-7, Jan. 2015.
- S. D. Stearns, “Incorrect stability criteria for non-Foster circuits”, in *Proceedings of the 2012 IEEE International Symposium on Antennas and Propagation.* IEEE, Jul 2012, pp. 1-2.
- M. Jacob, J. Long, and D. F. Sievenpiper, “Broadband non-Foster matching of an electrically small loop antenna”, in *2012 IEEE Antennas and Propag. Soc. Int. Symp. (APSURSI),* Jul. 2012, pp. 1-2.
- S. E. Sussman-Fort and R. M. Rudish, “Non-Foster impedance matching of electrically-small antennas”, vol. 57, no. 8, pp. 2230-2241, Aug. 2009.
- T. P. Weldon, J. M. C. Covington, K. L. Smith, and R. S. Adams, “Performance of digital discrete-time implementations of non-Foster circuit elements”, in *2015 IEEE International Symposium on Circuits and Systems (ISCAS),* May 2015, pp. 2169-2172.
- P. J. Kehoe, K. K. Steer, and T. P. Weldon, “Thevenin forms of digital discrete time non-Foster RC and RL circuits”, in *2016 IEEE International Symposium on Antennas and Propagation (APSURSI),* Jun 2016, pp. 191-192.
- M. H. Hayes, *Statistical Digital Signal Processing and Modelling,* 1st ed. John Wiley and Sons, Inc, 1996.